REMARKS

In the Final Office Action, the Examiner rejected claims 1, 2, 5-13, and 15. By the present Response, Applicants have not cancelled or added any claims. Applicants have amended claims 1 and 10 in view of a suggestion made by the Examiner. The present amendments do not add any new matter. In view of the following remarks, Applicants respectfully request reconsideration and allowance of all pending claims. Additionally, Applicants request that the Examiner address the incorrect indication of a final rejection in view of the new rejection and newly cited reference.

Interview Summary

The Applicants' representative, W. Allen Powell, conferred with the Examiner, James Mitchell, via telephone on November 2, 2009. Specifically, the Applicants' representative argued that the Final Office Action was improperly made final and that the claims are in condition for allowance. However, an agreement was not reached during the meeting. Applicants respectfully thank the Examiner for taking time to discuss the application.

Office Action Improperly Made Final

Applicants assert that the Office Action mailed on September 1, 2009, was improperly deemed "final" by the Examiner. No claims were amended and no new claims were added by the Response filed on May 5, 2009. Additionally, Applicants did not file an Information Disclosure Statement in the relevant time period. Despite this, while indicating a final rejection, the Examiner has added a new ground of rejection based on a newly cited reference. Specifically, by the Final Office Action mailed on September 1, 2009, the Examiner rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Ball (U.S. Patent No. 7,371,612) *in combination with Jeong et al.* (U.S. Patent Application No. 2006/0177954; hereafter "Jeong"). However, the Examiner had not previously submitted such a rejection.

Accordingly, the Final Office Action mailed on September 1, 2009, clearly should not have been designated as a final. Indeed, as set forth in M.P.E.P. § 706.07(a), "[u]nder present practice, second or any subsequent actions on the merits shall be final, *except where the examiner*

introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims, nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p)." (Emphasis added). Furthermore, the M.P.E.P. states that "a second or any subsequent action on the merits in any application or patent undergoing reexamination proceedings *will not be made final if it includes a rejection, on newly cited art,* other than information submitted in an information disclosure statement filed under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p), of any claim not amended by applicant or patent owner in spite of the fact that other claims may have been amended to require newly cited art." (Emphasis added).

Accordingly, in view of the clear error described above, Applicants respectfully request that the Examiner withdraw the finality of the Final Office Action mailed on September 1, 2009. Further, Applicants request that the Examiner respond to the present paper accordingly, and enter the amendment set forth above.

Claim Rejection Under 35 U.S.C. § 112, first paragraph

The Examiner rejected claims 1, 2, 5-13, and 15 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The Applicants respectfully traverse this rejection.

Regarding the enablement requirement, the Examiner has the initial burden to establish a *reasonable basis* to question the enablement provided for the claimed invention. *In re Wright*, 999 F.2d 1557, 1562, 27 U.S.P.Q.2d 1510, 1513 (Fed. Cir. 1993). The test for enablement, as set forth by the Supreme Court, is whether the experimentation needed to practice the invention is undue or unreasonable. *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916). A patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661, 18 U.S.P.Q.2d 1331, 1332 (Fed. Cir. 1991). The *undue experimentation* test essentially evaluates whether one of reasonable skill in the art can make or use the invention from the disclosures in the patent coupled with information known in the art without undue

experimentation. *U.S. v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 U.S.P.Q.2d 1217, 1223 (Fed. Cir. 1988). As long as the specification discloses at least one method for making and using the claimed invention that bears a *reasonable correlation* to the entire scope of the claim, then the enablement requirement of Section 112 is satisfied. *In re Fisher*, 427 F.2d 833, 839, 166 U.S.P.Q. 18, 24 (C.C.P.A. 1970).

As amended, independent claim 1 recites that each of a plurality of semiconductor die stacks comprises "at least two semiconductor die permanently coupled together by adhesive ... and wherein the plurality of semiconductor die stacks *are not mounted on a substrate*." (Emphasis added). Similarly, amended independent claim 10 recites that each of a plurality of semiconductor die stacks comprises "at least two semiconductor die coupled together by set adhesive that has been cured ... and wherein the plurality of semiconductor die stacks *are not mounted on a substrate*." (Emphasis added).

In rejecting independent claims 1 and 10, the Examiner stated the following:

> The definition of a substrate is a supporting material on or *in which* the components of an integrated circuit are *fabricated or attached*, or an insulating layer that components are formed on; therefore, since the dies contain circuits formed in semiconductor substrates the stack includes a substrate. *Alternatively, the die stacks are formed on/attached to a holder albeit temporarily and therefore the holder is still within the definition of a substrate.* As such, the claim is not enabled, since one skilled in the art to which it pertains, or with which it is most nearly connected, cannot make a stack formed on *what it excludes.*

Final Office Action, p. 2 (emphasis in original). Additionally, in the "Response to Arguments" portion of the Final Office Action, the Examiner stated that "Applicant's invention is really a die stack that is *not mounted on a substrate* this is different than a claim of a die stacks 'do not include a substrate'." Final Office Action, pp. 5-6 (emphasis in original). In view of this statement, Applicants amended claims 1 and 10 to facilitate prosecution by clarifying the

meaning of the recitation to the Examiner. Thus, Applicants believe the Examiner's concerns regarding this feature are addressed by the present amendment.

While Applicants believe the present amendment addresses the Examiner's concerns, in the event that the Examiner does not enter the amendment, Applicants assert that the Examiner's argument remains improper. Indeed, in arguing about the recitation "do not include a substrate," the Examiner provided an example that demonstrates that the Examiner is not interpreting the claims based on their plain meaning in view of the specification. Specifically, the Examiner asserted that "if the claim was a chip/die or die do not include a substrate, one of ordinary skill in the art would not be able to make the die, because the IC of a die are formed in or on a substrate." *Id.* p. 6. This clearly indicates that the Examiner is not interpreting the claim language in the proper context provided on the face of the claim. Further, the Examiner is certainly not interpreting the claim language in view of the specification or the standard terminology used in the relevant art. Indeed, the Examiner's argument is similar to asserting that a claim related to a brick building that excludes a building foundation is not enabled because each brick includes a so-called foundation, when the context of the claim language and the specification makes it plain that references to a foundation are directed to a building foundation, not *anything* on which something can be placed. Despite the clear context provided on the face of the claim and supported throughout the application, the Examiner is not considering the context of a die *stack*. Rather, the Examiner is improperly focusing on each individual die.

Regarding the enablement requirement of 35 U.S.C. § 112, first paragraph, Applicants assert that one of ordinary skill in the art would clearly understand how to form a die *stack without a substrate* or a die *stack not mounted on a substrate* based on the disclosure of the present application. *See, e.g.*, Application, p. 17, line 16 – p. 18, line 11. Indeed, this concept is discussed in great detail throughout the application and distinguishes present embodiments from prior art in which packages are assembled by sequentially stacking die directly on a substrate. For example, in various places throughout the present application, a temporary holding surface is contrasted with a substrate. *See, e.g.*, p. 12, lines 15-17. Thus, contrary to the Examiner's

assertions that a substrate may include a temporary holding surface, the specification makes it clear that a temporary holding surface is not a substrate. *See* Final Office Action, pp. 2 and 6.

In the Office Action, the Examiner apparently asserted that a die stack inherently includes a substrate. *See* Final Office Action, p. 2. Indeed, on page 6 of the Final Office Action, the Examiner stated that "every die includes a substrate." Again, Applicants stress that the Examiner is taking the recited terms out of the context provided by the claims and the specification. Specifically, as set forth above, the Examiner provided his own definition of a substrate by stating that "[t]he definition of a substrate is a supporting material on or *in which* the components of an integrated circuit are *fabricated or attached*, or an insulating layer that components are formed on." Final Office Action, p. 2 (emphasis in original). The Examiner did not provide a specific source for this definition. However, the Examiner did previously point to Gerritsen et al. (U.S. Pub. No. 2003/0207569) (hereafter referred to as "the Gerritsen reference") as support for the Examiner's apparent assertion that because the recited "die stack" of claims 1 and 10 includes individual die that the "die stack" necessarily includes a substrate, which will be discussed below. *See* Office Action mailed February 5, 2009, p. 6. Additionally, in the Final Office Action, the Examiner asserted that "Examiner's definition is explicit in the USPTO class definition section along with countless references or articles dealing with chip manufacture, while applicant has merely relied on conjecture that is insufficient." Final Office Action, p. 6. However, it should first be noted that Applicants's arguments are not based on conjecture but on the plain meaning of the claim terms within the context of the claim and the specification. Additionally, Applicants assert that there is no legal precedent that stands for the position that class definitions provided by the U.S.P.T.O. should be considered over the specification in interpreting claim language. Indeed, Applicants remind the Examiner that the claim terms are to be interpreted *in view of the specification*. It is inappropriate for the Examiner to simply make up his own definition, regardless of whether the Examiner utilized U.S.P.T.O. documents to make up the definition. Likewise, as will be discussed below, the Gerritsen reference should not be used to interpret the claim terms over the specification. Indeed, the Gerritsen reference is not even directed to the same specific area of technology as that of the present application.

With regard to the definition supplied by the Examiner of a "substrate" and the Examiner's general use of the Gerritsen reference and the U.S.P.T.O. class definitions to interpret the meaning of a "substrate" in the present claim recitations, Applicants note that they are well aware that *some* definitions of a "substrate" are quite broad. However, Applicants stress that the English language is limited, and, thus, certain identical terms may be used in different contexts (e.g., different areas of technology) to provide different meanings. These limitations on language were likely contemplated by the courts when they established the precedent that requires claims to be interpreted in view of the specification. Indeed, according to legal precedent, during patent examination, the pending claims must be given their broadest *reasonable* interpretation *consistent* with the specification. *See In re Prater*, 415 F.2d 1393, 1404-05, 162 U.S.P.Q. 541, 550-51 (C.C.P.A. 1969); *see also In re Morris,* 127 F.3d 1048, 1054-55, 44 U.S.P.Q.2d 1023, 1027-28 (Fed. Cir. 1997); *see also* M.P.E.P. §§ 608.01(o) and 2111. Further, interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *See In re Cortright*, 165 F.3d 1353, 1359, 49 U.S.P.Q.2d 1464, 1468 (Fed. Cir. 1999); *see also* M.P.E.P. § 2111. Thus, Applicants assert that the Examiner's attempt to provide his own definition of the term "substrate" was improper. Further, the Examiner should not attempt to define the meaning of claim terms in the present application based on other references. Indeed, Applicants assert that sufficient context has clearly been provided by the present specification for an appropriate interpretation of the term "substrate."

With regard to the Examiner's assertions based on the U.S.P.T.O. website, Applicants note that, as discussed above, there are numerous uses of the term "substrate" in the English language and proper interpretation is dependent upon context. This assertion is only supported by a brief review of www.uspto.gov/web/patents/classifications/uspc257/defs257.htm, which was cited by the Examiner. Indeed, the cited website makes it very clear that the context of the term provides meaning. With regard to the Examiner's assertions based on the Gerritsen reference, Applicants assert that the Gerritsen reference is generally directed to a process for forming microelectronic devices or integrated circuits (e.g., CMOS and PMOS devices). Specifically, the

Gerritsen reference is directed to forming certain features (i.e., layers) of an integrated circuit, which may generally be referred to as a "die." In the Gerritsen reference, the surface on which layers are formed is referred to as a "silicon semiconductor *substrate*." *Id.*, Abstract (emphasis added). Based on this disclosure, the Examiner apparently asserted that the recited die stacks of claims 1 and 10 include substrates. However, Applicants stress that the Gerritsen reference is directed to forming *die*. In contrast, the present application is directed to stacking die that have already been formed. In other words, the present application is directed to forming *die stacks*. There is a clear issue of scale. Thus, the Gerritsen reference is essentially in a different area of technology than the claims of the present application. When forming die stacks, the term "substrate" has a completely different meaning than it would in a process for forming a die. Accordingly, Applicants assert that it was improper for the Examiner to look to a reference directed to forming *die* in order to interpret a term used in an application directed to forming *die stacks*. Indeed, based on the legal precedent set forth above, rather than look to other references, the Examiner should have simply considered the context provided by the present specification and the claim language itself.

The claim language set forth in claims 1 and 10, on its face, clearly indicates that the die stacks *do not include* or *are not mounted on* substrates. Additionally, the specification clearly indicates that die stacks are eventually *stacked on* a substrate to form a package. They are not *integral with* the substrate. Further, the term "substrate" has a well known meaning in the art. *Based on the context in which the term is utilized in the specification*, one of ordinary skill in the art would readily discern the intended meaning. For example, the die stacks are described as being coupled to the substrate to form a package, such as the packages illustrated in FIGS. 2 and 3 of the application. *See e.g.,* Application, page 18, lines 9-11. Prior to coupling the die stacks to the substrate, the die stacks do not include a substrate, and certainly do not form a package.

In summary, the Examiner's assertion that one of ordinary skill in the art would be confused about the meaning of the term "substrate" is unfounded. Indeed, Applicants assert that based on the context in which the term "substrate" is used in the claims and the specification and

based on the customary meaning of the term in the art, one of ordinary skill in the art would clearly understand the intended meaning. Further, Applicants assert that any confusion with respect to this claim feature merely arose because the Examiner attempted to provide his own unreasonably broad definition for the term and looked to other areas of technology for support. Those skilled in the art would not make such an interpretation, nor would they be confused as to how to make or use the invention, as recited in the present claims.

Second, the Examiner apparently asserted that the temporary holding surface is a substrate. *See* Final Office Action, pp. 2 and 6. Again, this is clearly not the case. As set forth above, the term "substrate" has a well known meaning in the art. The definition that is apparently being asserted by the Examiner is unreasonably broad. Indeed, according to the Examiner it seems that anything on which a die stack is placed can be interpreted as a substrate. This clearly does not fit with the customary meaning of the term or the meaning of the term based on the context of its use throughout the present application. For example, as set forth in the present application, attaching a substrate to a die stack forms a package. *See e.g.,* Application, p. 17, line 16 – page 18, line 11. However, when a die stack is placed on a temporary holding surface, a package is not formed. Attachment to a substrate is clearly understood by those skilled in the art to connote a permanent attachment, rather than a temporary placement.

In view of the remarks set forth above, Applicants assert that independent claims 1 and 10, as well as those claims dependent thereon, are fully compliant with the requirements of 35 U.S.C. § 112, first paragraph. Accordingly, Applicants request that the Examiner withdraw the rejection of claims 1, 2 and 5-15 under 35 U.S.C. § 112, first paragraph, and provide an indication of allowance for claims 1, 2 and 5-15.

Claim Rejections Under 35 U.S.C. § 102

In the Final Office Action, the Examiner rejected claims 1, 5, 9-11, and 15 under 35 U.S.C. § 102(e) as being anticipated by Ball (U.S. Patent No. 7,371,612) (hereafter referred to as "the Ball reference"). Applicants respectfully traverse this rejection.

Anticipation under 35 U.S.C. § 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). That is, to maintain a proper rejection under 35 U.S.C. § 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Indeed, the cited reference must not only disclose all of the recited features but must also disclose the part-to-part relationships between the features. *See Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 U.S.P.Q. 481, 486 (Fed. Cir.1984). Accordingly, the Applicants need only point to a single element or claimed relationship not found in the cited reference to demonstrate that the cited reference fails to anticipate the claimed subject matter.

Embodiments of the present disclosure are directed to one or more *die stacks* that are deposited on a temporary holding surface in a *completed* form. *See* Application, page 12, lines 11-13. For example, using a stacking tip, a completed die stack may be positioned on a temporary holding surface (e.g., a film frame, gel pack, tape reel, or JEDEC tray) for later attachment onto a substrate. *See id.* Thus, the temporary holding surface is configured to temporarily hold the completed die stack for eventual transfer to a permanent coupling with a substrate. For example, the temporary holding surface may facilitate removal of a completed die stack from the temporary holding surface with a stacking tip. The die forming a completed die stack may be permanently coupled together in the stacked formation prior to moving the die stack from the temporary holding surface to the substrate. For example, the

die stack may be cured at a high temperature prior to moving the die stack from the temporary holding surface to the substrate, wherein the curing may set adhesive between die of the die stack to permanently couple the die in the stack together. *See id.*, page 10, lines 1-2 and page 12, lines 13-15. Additionally, prior to attachment to the substrate, the die may be tested to ensure that all die in the stack are functional, thus forming a known good die stack. *See id.*, page 12, lines 15-17. Applicants stress that the present application refers to a known good *die stack* (KGDS), not merely a known good die (KGD). In other words, *a completed die stack* has been tested and is known to be good, thus, becoming a known good die stack and not merely a single and separate known good die.

Accordingly, as amended, independent claim 1 recites, *inter alia*, "A temporary holding surface having a plurality of die stacks thereon ... wherein each of the plurality of semiconductor die stacks comprises at least two semiconductor die permanently coupled together, wherein the stack of at least two semiconductor die comprises a *known good die stack*, and wherein the plurality of semiconductor die stacks are not mounted on a substrate." (Emphasis added). As amended, independent claim 10 recites, *inter alia*, "[a] tape reel having a plurality of semiconductor die stacks thereon ... wherein each of the plurality of semiconductor die stacks comprises at least two semiconductor die coupled together by set adhesive that has been cured, wherein each of the plurality of semiconductor die stacks comprises a *known good die stack*, and wherein the plurality of semiconductor die stacks are not mounted on a substrate." (Emphasis added).

In contrast, the Ball reference fails to disclose a temporary holding surface or a tape reel having a plurality of die stacks thereon, wherein each of the die stacks comprises a *known good die stack*, as recited in amended claims 1 and 10. However, in the Office Action, the Examiner apparently asserted that the Ball reference discloses a known good die or KGD because is discloses testing a wafer, and then the Examiner asserted that one KGD could be positioned on another KGD. *See* Final Office Action, page 3. Apparently, by making this assertion, the Examiner intended to assert that Ball discloses a known good die *stack* or KGDS. Indeed, in the Response to Arguments

portion of the Final Office Action, the Examiner stated that "[a] claim of a KGD die stack [sic] is not limited as applicants contend to a stack that has been tested while in a stack configuration rather than two attached, stacked KGD [sic] are encompassed within the broad claim of KGD die stack." Final Office Action, pages 6-7.

First, Applicants assert that the Ball reference is clearly insufficient to support a rejection under 35 U.S.C. § 102 because it does not disclose a known good die *stack*. At best, the Examiner apparently believes that is would be obvious to stack two KGD on one another. Second, Applicants do not understand where the Examiner is getting the interpretation of a KGDS being asserted by the Examiner in the Final Office Action. Indeed, the plain language of the claim recitations clearly indicates that the recited "stack" and "stacks" include a "known good die stack," *not* a stack of known good die. There is clearly a distinction between the meanings of these phrases. Indeed on the face of the claim language, a "known good die stack" describes an entire stack, not merely parts within a stack. Further, the Applicants again remind the Examiner that the claim terms are to be interpreted *in view of the specification*. Also, Applicants stress that specification clearly contradicts the interpretation suggested by the Examiner. Indeed, a KGDS is discussed as follows in the specification:

> Once the die stack is formed, the *completed die stack* may be deposited on a temporary holding surface … prior to attachment to a substrate or even prior to attachment to the temporary holding surface, the die may be tested to ensure that all die *in the stack* are functional, *thus forming a known good die stack (KGDS).*

Application, p. 12, lines 11-17 (emphasis added). Thus, Applicants assert that a known good die stack or KGDS clearly refers to a *completed* die stack that has been tested and determined to be functional. A KGDS is *not* merely a stack of individually tested die, as suggested by the Examiner. Indeed, Applicants stress that just because a stack includes a KGD, it does not necessarily constitute a KGDS. While all of the die in a die stack may have been tested, the stack itself may not function and certainly may not be a known good die stack. Accordingly, because the Ball reference is

deficient is this regard and clearly does not disclose all of the recited features of claims 1 and 10, Applicants assert that the Ball reference cannot anticipate independent claims 1 and 10.

The Examiner also apparently argued that because a KGDS, in accordance with present embodiments, may be damaged at a later time, that this somehow impacts patentability. Specifically, the Examiner stated the following:

> [A]pplicant has already indicated that his die stack does not have a permanent substrate; hence, the stack is not in a permanent package and still subject to being defective in subsequent processing. When applicant's chips are moved to permanent substrate he only has two functional dies that make up his KGD stack, which is the same structure as in prior art.

Final Office Action, p. 7. Applicants do not fully understand the Examiner's position quoted above. However, Applicants stress that the mere fact that a KGDS could be damaged at some point in the future is not a reason for rejecting the claims.

In summary, Applicants assert that the Examiner has provided no indication of where the Ball reference allegedly discloses a known good die *stack* or KGDS. At best, the Examiner has merely asserted that the Ball reference discloses a single KGD and has suggested that separately tested die may be stacked on top of one another. Thus, the Ball reference fails to disclose all of the recited features of claims 1 and 10. Additionally, Applicants note that the Examiner essentially relied on the figures of the Ball reference as support. Accordingly, Applicants respectfully remind the Examiner that the *drawings* of the cited reference must be evaluated for what they *reasonably disclose and suggest* to one of ordinary skill in the art. *In re Aslanian*, 590 F.2d 911, 200 U.S.P.Q. 500 (C.C.P.A. 1979). Drawings and pictures can anticipate claims if they clearly show the structure which is claimed. *In re Mraz*, 455 F.2d 1069, 173 U.S.P.Q. 25 (C.C.P.A. 1972). However, the picture must show all the claimed structural features and how they are put together. *Jockmus v. Leviton*, 28 F.2d 812 (2d Cir. 1928).

For at least the reasons set forth above, Applicants respectfully request that the Examiner withdraw the rejection under 35 U.S.C. § 102 and provide an indication of allowance for independent claims 1 and 10. Additionally, based on their dependence from an allowable base claim and for unique features recite in each claim, Applicants assert that the claims depending from claims 1 and 10 should also be allowed.

Claim Rejections Under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected claims 2, 6, 7, 12 and 13 under 35 U.S.C. § 103(a) as being unpatentable over the Ball reference in combination with Jeong et al. (US 2006/0177954). Applicants respectfully traverse this rejection.

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). However, it is not enough to show that all the elements exist in the prior art since a claimed invention composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. *KSR International Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741 (2007). It is important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. *Id.* Specifically, there must be some articulated reasoning with a rational underpinning to support a conclusion of obviousness; a conclusory statement will not suffice. *In re Kahn,* 441 F.3d 977, 988 (Fed. Cir. 2006). Indeed, the factual inquiry determining whether to combine references must be thorough and searching, and it must be based on *objective evidence of record. See In re Lee,* 61 U.S.P.Q.2d 1430, 1436 (Fed. Cir. 2002).

Applicants note that all of the claims rejected under 35 U.S.C. § 103 are each dependent (directly or indirectly) on either independent claim 1 or independent claim 10. Thus, each of the claims rejected under 35 U.S.C. § 103 depend from a claim rejected under 35 U.S.C. § 102,

based on the Ball reference. As discussed above, the Ball reference does not disclose each and every feature recited in independent claims 1 and 10. Further, the Examiner's mere assertions of obviousness and official notice do not remedy the deficiencies of the Ball reference. As such, the Ball reference, whether considered alone or in conjunction with the Examiner's assertions, is not believed to render the presently pending claims obvious. Accordingly, in view of the arguments set forth above, Applicants respectfully request that the Examiner withdraw each of the rejections under 35 U.S.C. § 103 and provide an indication of allowance for claims 2, 6, 7, 12 and 13.

Payment of Fees and General Authorization for Extensions of Time

No fees are believed to be due at this time. If any fees, including fees for extensions of time and other reasons, are deemed necessary to advance prosecution of the present application, at this or any other time, Applicants hereby authorize the Commissioner to charge such requisite fees to Deposit Account No. 06-1315; Order No. MICS:0078-5. In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request thereof.

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully request allowance of the pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: November 2, 2009

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